## REMARKS

The Examiner is thanked for his thorough inspection of the application papers and their conformity with current USPTO practice. Before entry of this amendment, claims 1-21 were pending. In the Office Action, claims 1-4, 7-8 and 20 were rejected, and claims 5-6 were objected to. Claims 9-19 and 21 are allowed. In the present amendment, claims 1, 5-6 and 19-20 are amended. After entry of the amendment, claims 1-21 are pending.

Reconsideration and allowance is respectfully requested.

### I. Claim Objections

Claims 1 and 19 are objected to because they contain the word "if" as opposed to the positive limitation "when." (See Office Action, p. 2, lines 13-16.) The appropriate correction has been made to claim 1, line 7, and to claim 19 lines 8 and 10. Withdrawal of the objection to claims 1 and 19 is respectfully requested.

Claims 5 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. (See Office Action, p. 4, lines 17-19.) Applicants amend claims 5 and 6 to include all of the limitations of the base claim 1 and the intervening claim 4. Withdrawal of the objection to claims 5 and 6 is respectfully requested.

### II. Rejection of claims 1-4, 7-8 and 20

Claims 1-4, 7-8 and 20 are rejected under 35 U.S.C. §102(e) as being anticipated by Hirai (US Pub No. 2002/0180540) (Office Action, p. 3, lines 6-7). The Examiner cites the appropriate paragraph of §102 that forms the basis of the §102 rejection as:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States . . . or on an international application by another . . .. (Office Action, p. 2, lines 20-23)

Hirai is not prior art under the version of §102(e) that is the basis for the rejection because Hirai is not a granted patent. Moreover, Hirai does not disclose all of the claim limitations recited in claims 1-4, 7-8 and 20.

A. Independent claim 1

The Examiner states, with regard to claim 1, that "Hirai discloses, in Figure 1, a circuit and its corresponding method comprising the steps of a) determining [11] a cycle period of first clock signal [reference signal]; b) detecting [11] rising and falling edges of a second clock signal [feedback signal] during the cycle period the first clock signal; and c) designating the cycle period of the first clock signal as valid when a single rising edge of the second clock signal and a single falling edge of the second clock signal are detected during the cycle period of the first clock signal *(this occurs during the lock condition)*." (Office Action, p. 3, lines 8-14, italics in original). Applicants respectfully disagree.

Hirai does not form the basis for a valid rejection under § 102(e) because Hirai does not disclose all three of the elements of claim 1 cited by the Examiner. For example, Hirai does not disclose the third element recited in claim 1:

> "designating the cycle period of the first clock signal as valid when a single rising edge of the second clock signal and a single falling edge of the second clock signal are detected during the clock period of the first clock signal."

The Examiner points to nothing in Hirai that discloses designating any particular cycle of the reference clock as being valid. The lock detection circuit of Hirai does not detect when a particular cycle of the first clock signal is valid. Instead,

Hirai detects a locked state by comparing a number of counted feedback signal cycles to a number of counted of reference signal cycles. Hirai states:

> "The first counter 21 counts up on the rising edge of the inputted feedback signal. The second counter 22 counts up on the rising edge of the inputted reference signal." (Hirai at ¶ [0034])
>
> ". . . The first counter 21 and the second counter 22 successively count the feedback signals by the number of cycles by NAxC (corresponding to a period of tCKxNAxC when a cycle of the feedback signal is tCK). . . . For the NA and C values, an optional combination of 16 and 256, 256 and 8 and the like can be applied . . ." (Hirai at ¶ [0042])
>
> ". . . An unlock state can be detected in each NA cycle of the feedback signal." (Hirai at ¶ [0063])
>
> ". . ., the present invention has at least a first and a second counters for counting feedback signals and reference signals and a third counter for counting the number of coincidences of the set values in the first and second counters. . . ." (Hirai at ¶ [0063])

Hirai does not disclose designating a cycle of the reference clock as being valid, but rather compares a number of feedback signal cycles to a number of reference signal cycles. Although the third counter of Hirai does count falling edges of the feedback signal, Hirai does not detect a locked state when a single rising edge and a single falling edge of the feedback clock occur during particular cycles of the reference clock. Thus, Hirai indicates frequency lock based on the average frequencies of the feedback and reference clock signals over a period of time, as opposed to indicating a locked state based on a predetermined number of consecutive valid cycles.

Because Hirai does not disclose all of the elements of claim 1, reconsideration of the § 102(e) rejection and allowance of claim 1 is requested.

B. Dependent claims 2-4 and 7-8

Claims 2-4 and 7-8 depend from claim 1.

Dependent claim 2 is rejected as being anticipated by Hirai. (Office Action, p. 3, lines 15-16.) Claim 2 depends from claim 1, and Applicants respectfully submit that claim 2 is allowable for at least the same reasons for which claim 1 is allowable. Reconsideration and allowance of claim 2 is requested.

Dependent claim 3 is rejected as being anticipated by Hirai. The Examiner states, with regard to claim 3, that "Hirai discloses, in Figure 1, that the determining the cycle period of the first clock signal further comprises detecting [11] a rising edge of the first clock signal and detecting [11] an immediately following rising edge the first clock signal." (Office Action, p. 3, lines 17-19.) Applicants disagree. Hirai does not disclose determining a cycle period by detecting a rising edge and an immediately following rising edge of a clock signal. Although two counters of Hirai count up on rising edges of clock signals, Hirai does not disclose a means for determining a cycle period between a rising edge and an immediately following rising edge. Hirai does not disclose a means for determining a cycle period of a first clock signal during which a rising or falling edge of a second clock signal might occur, for example, a period after a rising edge and before an immediately following rising edge of the first clock signal.

Because Hirai does not disclose all of the elements of claim 3, reconsideration of the § 102(e) rejection and allowance of claim 3 is requested. In addition, claim 3 depends from claim 1 and is allowable for at least the same reasons for which claim 1 is allowable. Reconsideration and allowance of claim 3 is requested.

Dependent claim 4 is rejected as being anticipated by Hirai. The Examiner states, with regard to claim 4, that "Hirai discloses, in Figure 1, that the method further comprises the step of counting [22] a number of consecutive cycle periods of the first clock signal that are designated as valid." (Office Action, p. 3, lines 20-22.) Applicants disagree. Hirai does not disclose counting valid cycle periods. Counter 22 of Hirai simply counts a predetermined number of cycles regardless of whether each cycle is valid. Only after the predetermined number of cycles

are counted and compared does the circuit of Hirai determine whether two signals are locked or unlocked.

> "The decision circuit (25) outputs a signal showing an unlock stated when the count value of the first counter (21) reaches a predetermined first value and the count value of the second counter (22) is different from the first value. . . ." (Hirai at ¶ [0030])
>
> ". . . The first counter 21 and the second counter 22 successively count the feedback signals by the number of cycles by NAxC (corresponding to a period of tCKxNAxC when a cycle of the feedback signal is tCK). . . . For the NA and C values, an optional combination of 16 and 256, 256 and 8 and the like can be applied . . ." (Hirai at ¶ [0042])

Reconsideration of the § 102(e) rejection and allowance of claim 4 is requested because Hirai does not disclose all of the elements of claim 4. In addition, claim 4 depends from claim 1 and is allowable for at least the same reasons for which claim 1 is allowable. Reconsideration and allowance of claim 4 is requested.

Dependent claim 7 is rejected as being anticipated by Hirai. The Examiner states, with regard to claim 7, that "Hirai discloses, in Figure 1, that designating the cycle period of the first clock signal as valid further comprises detecting [11] a single rising edge of a skewed *(skewed since having to propagate through components such as [12,13,14] along the feedback path)* second clock signal and a single falling edge of the skewed second clock signal during a subsequent cycle period the first signal." (Office Action, p. 4, lines 1-5, italics in original.) Applicants disagree. Hirai does not disclose designating a clock cycle as valid. Moreover, the counters [21,22,24] of the lock detection circuit [20] of Hirai count edges of only two signals: a reference signal and a feedback signal. Hirai does not disclose a third signal for which edges are detected. Thus, Hirai does not disclose a skewed second clock signal in addition to a first clock signal and a second clock signal.

Because Hirai does not disclose all of the elements of claim 7, reconsideration of the § 102(e) rejection and allowance of claim 7 is requested. In addition, claim 7 depends from claim 1 and is allowable for at least the same reasons for which claim 1 is allowable. Reconsideration and allowance of claim 7 is requested.

Dependent claim 8 is rejected as being anticipated by Hirai. (Office Action, p. 4, lines 6-9.) Claim 8 depends from claim 1, and Applicants respectfully submit that claim 8 is allowable for at least the same reasons for which claim 1 is allowable. Reconsideration and allowance of claim 8 is requested.

C. Independent claim 20

Claim 20 is rejected under 35 U.S.C. § 102(e) as being anticipated by Hirai. In response, Applicants have amended claim 20 to recite:

> "means for detecting when the feedback clock signal and the reference clock signal are out of lock, wherein the means detects that the feedback clock signal and the reference clock signal are out of lock when a like number of feedback clock cycles and reference clock cycles occur during a time period and when a single rising edge and a single falling edge of the feedback clock signal are detected during less than a predetermined number of the reference clock cycles during the time period."

The rejection of claim 20 under § 102(e) should be withdrawn in light of the foregoing amendment because Hirai does not disclose all of the limitations of amended claim 20.

Hirai does not disclose a means for detecting that a rising edge and falling edge of a feedback clock signal occur during a reference clock cycle. Hirai does not disclose a means for detecting an out of lock state when the same number of feedback clock cycles and reference clock cycles occur during a time period. Rather, Hirai compares a number of feedback signal cycles to a number

of reference signal cycles that are counted during a time period and indicates that the feedback clock signal and the reference clock signal are locked when the same number of feedback clock cycles and reference clock cycles occur during that time period. Applicants respectfully submit that claim 20 is in a condition for allowance.

VI. Conclusion

In view of the foregoing amendments and remarks, Applicants respectfully submit that the entire application (claims 1-21 are pending) is in condition for allowance. Moreover, Applicants maintain that claims 1-21 are valid over art in addition to Hirai cited in the "Citation of Relevant Prior Art." Applicants respectfully request that a timely Notice of Allowance be issued in this case. If the Examiner would like to discuss any aspect of this application, the Examiner is requested to contact the undersigned at (925) 621-2121.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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